Amendments to the Claims

Following is a listing of the claims, which will replace all prior versions and listings of claims in this application:

Listing of the Claims

Claims 1-17 (Canceled)

18. (Currently Amended) A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components provided on a circuit surface, one of the first and second chips comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a first electrode provided in the first wiring layer; and

a plurality of second electrodes provided on each of the conductive lines, the conductive lines being configured to interconnect the first electrode and the plurality of second electrodes,

wherein the plurality of second electrodes are provided such that, when the first and second chips are combined together, the plurality of second electrodes contact corresponding electrodes of the other of the first and second

chips so that the conductive lines interconnect the first chip and the second chip via the plurality of second electrodes,

wherein the first chip and the second chip are disposed so that the circuit surface of the first chip and the circuit surface of the second chip confront each other.

19. (Currently Amended) A multi-chip semiconductor apparatus in which a plurality of chips coexist and each of the plurality of chips includes circuit components provided on a circuit surface, comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a plurality of first electrodes provided in the first wiring layer; and

a plurality of second electrodes provided on each of the conductive lines, the conductive lines being configured to interconnect the plurality of first electrodes and the plurality of second electrodes,

wherein the first chip and the second chip are disposed so that the circuit surface of the first chip and the circuit surface of the second chip confront each other.

20. (Currently Amended) A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second

chips includes circuit components provided on a circuit surface, the first chip comprising:

a first wiring layer provided on a first semiconductor substrate;

a second wiring layer provided on a first insulating layer covering the first wiring layer, the second wiring layer including first conductive lines each interconnecting the circuit components of the first chip;

a first electrode provided in the first wiring layer; and

a second electrode provided on each of the first conductive lines, each first conductive line being configured to interconnect the first electrode and the second electrode,

the second chip comprising:

a third wiring layer provided on a second semiconductor substrate;

a fourth wiring layer provided on a second insulating layer covering the third wiring layer, the fourth wiring layer including second conductive lines each interconnecting the circuit components of the second chip;

a third electrode provided in the third wiring layer; and

a fourth electrode provided on each of the second conductive lines, the fourth electrode being arranged such that, when the first and second chips are combined together, the four electrode contacts the second electrode,

wherein the first chip and the second chip are disposed so that the circuit surface of the first chip and the circuit surface of the second chip confront each other.

21. (Currently Amended) A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components provided on a circuit surface,

the first chip comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of the first chip;

a first electrode provided in the first wiring layer; and

a second electrode provided on each of the conductive lines, each conductive line being arranged to interconnect the first electrode and the second electrode,

the second chip comprising:

a plurality of third electrodes which are arranged such that, when the first and second chips are combined together, the plurality of third electrodes contact the respective second electrodes of the first chip to interconnect the respective conductive lines of the first chip,

wherein the first chip and the second chip are disposed so that the circuit surface of the first chip and the circuit surface of the second chip confront each other.

Claims 22-29 (Canceled)

30. (Original) The semiconductor apparatus according to claim 19, wherein the plurality of chips include a memory chip and a logic chip.

Claims 31-41 (Canceled)